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10/712,473	11/12/2003	Robert E. Ober	20658/0203692-US0	9335

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,473	OBER ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22, 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-22, and 24-36 have been examined.

Acknowledgment of papers filed: amendments and remarks filed on May 8th, 2006. The papers filed have been placed on record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 9-16, 20-22, 24-26, 29-32 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Hobbs (U.S. Patent No. 5,197,138).

4. Regarding claim 1, Hobbs discloses a method for operating a multi-threaded system having a plurality of active threads (col 1 lines 63-66), the method comprising: assigning an interrupt priority value to each of a plurality of interrupts (col 2 lines 46-50); specifying an interrupt threshold value; and processing a requested interrupt only when the interrupt priority value of the requested interrupt is higher than the interrupt threshold value (col 2 lines 54-57).

5. Regarding claim 2, Hobbs discloses the method of claim 1, wherein processing the requested interrupt comprises: performing an interrupt entry process to prepare for

an interrupt service routine (ISR); executing the ISR (col 2 lines 6-13); and performing an interrupt exit process to return control from the ISR (col 2 lines 14-19).

6. Regarding claim 3, Hobbs discloses the method of claim 2, wherein performing the interrupt entry process comprises: identifying one of the plurality of active threads as an interrupt thread; switching to the interrupt thread if the interrupt thread is not executing (col 2 line 67 to col 3 line 3); and branching to the ISR (col 2 lines 6-13).

7. Regarding claim 4, Hobbs discloses the method of claim 3, wherein each of the plurality of active threads comprises a thread context, and wherein performing the interrupt entry process further comprises saving the thread context of the interrupt thread (col 1 lines 57-64).

8. Regarding claim 5, Hobbs discloses the method of claim 4, wherein performing the interrupt exit process comprises: executing a return from exception (RFE) instruction (col 2 lines 14-19); and restoring the thread context of the interrupt thread (col 1 lines 60-63).

9. Regarding claim 9, Hobbs discloses the method of claim 3, wherein each of the plurality of active threads consists of a first set of context registers (col 1 lines 60-63) and a second set of context registers (col 1 lines 60-63),

Note that the saving of the context registers is unique for each thread. The use of multiple threads (col 1 lines 63-66) suggests a second set of context registsers.

Wherein performing the interrupt entry process further comprises saving the first set of context registers of the interrupt thread (col 1 lines 60-63), and wherein executing the ISR comprises: saving the second set of context registers of the interrupt thread if the second set of context registers of the interrupt thread are required for servicing the requested interrupt (col 1 lines 60-63); servicing the requested interrupt (col 2 lines 12-14); and restoring the second set of context registers of the interrupt thread after servicing the requested interrupt if the second set of context registers of the interrupt thread were required for servicing the requested interrupt (col 2 lines 14-19).

10. Regarding claim 10, Hobbs discloses the method of claim 9, wherein performing the interrupt exit process comprises: executing a return from exception (RFE) instruction (col 2 lines 6-13); and restoring the upper context registers of the interrupt thread (col 2 lines 14-19).

11. Regarding claim 11, Hobbs discloses the method of claim 1, further comprising processing traps only in the active threads originating the traps (col 2 lines 22-32).

Note that all the instances provided refer to responding to traps in the active threads that originate the trap.

12. Regarding claim 12, Hobbs discloses the method of claim 11, wherein processing traps comprises: detecting a trap from an originating thread, the originating thread being one of the plurality of active threads (col 3 lines 7-10); storing trap background data for the trap if the trap is asynchronous (col 3 lines 24-29); and associating a trap pending indicator with the originating thread if the originating thread is not executing (col 3 lines 40-50).

Note in line 44 the use of the term "delay". This suggests that there is an indicator waiting for a change to the originating thread.

13. Regarding claim 13, Hobbs discloses the method of claim 12, wherein processing traps further comprises: performing a trap entry process to prepare for a trap handling routine (col 3 lines 40-50); executing the trap handling routine (col 2 lines 12-14); and performing a trap exit process to return control from the trap handling routine (col 2 lines 14-19).

Note that, in col 3 line 48, it is stated that an I/O interrupt routine is used for the trap, indicating that a trap uses the same methods for handling as typical interrupts.

14. Regarding claim 14, Hobbs discloses the method of claim 13, wherein each of the plurality of active threads comprises a thread context (col 1 lines 63-66), and wherein performing the trap entry process comprises: waiting for originating thread to start executing if the originating thread is not executing (col 2 line 67 to col 3 line 3);

saving the thread context of the originating thread (col 2 lines 6-13); and branching to a trap handler (col 2 lines 12-14).

15. Regarding claim 15, Hobbs discloses the method of claim 14, wherein waiting for the originating thread to start executing comprises monitoring the plurality of active threads until execution switches to one of the plurality of active threads associated with the trap pending indicator (col 3 lines 40-50).

16. Regarding claim 16, Hobbs discloses the method of claim 14, wherein performing the trap exit process comprises: executing a return from trap instruction; and restoring the context of the originating thread (col 2 lines 14-19).

Note, again, that a trap is handled as an interrupt.

17. Regarding claim 20, Hobbs discloses the method of claim 13, wherein each of the plurality of active threads consists of a first set of context registers (col 1 lines 60-63) and a second set of context registers (col 1 lines 60-63),

Note that the saving of the context registers is unique for each thread. The use of multiple threads (col 1 lines 63-66) suggests a second set of context registsers.

Wherein performing the trap entry process further comprises saving the first set of context registers of the originating thread (col 2 lines 7-12), and wherein executing the trap handling routine comprises: saving the second set of context registers of the

originating thread if the second set of context registers of the originating thread are required for servicing the trap (col 3 lines 40-50);

Note that, as explained in the citation, a context switch may be necessary which, as indicated in col 1 lines 57-63, requires saving the context into memory.

Servicing the trap (col 2 lines 12-14); and restoring the second set of context registers of the originating thread after servicing the trap if the second set of context registers of the interrupt thread were required for servicing the trap (col 2 lines 15-19).

18. Regarding claim 21, Hobbs discloses the method of claim 20, wherein performing the interrupt exit process comprises: executing a return from trap instruction; and restoring the upper context registers of the originating thread (col 2 lines 15-19).

19. Regarding claim 22, Hobbs discloses a method for operating a multi-threaded system having a plurality of active threads (col 1 lines 63-66), the method comprising: accepting a request for an interrupt; switching execution to a predetermined one of the plurality of active threads (col 2 line 67 to col 3 line 3); and executing an interrupt service request from the predetermined one of the plurality of active threads to service the interrupt (col 2 line 12-14).

20. Also regarding claim 22, Hobbs discloses the method of claim 22, wherein accepting a request for an interrupt comprises: assigning a unique interrupt priority value to each interrupt for the multi-threaded embedded system (col 2 lines 47-50);

specifying a common threshold interrupt value for all the active threads; and taking the interrupt only when the unique interrupt priority value of the interrupt is higher than the common threshold interrupt value (col 2 lines 54-57).

21. Regarding claim 24, Hobbs discloses a method for operating a multi-threaded embedded system having a plurality of active threads (col 1 lines 63-66), the method comprising processing traps only in the active threads originating the traps (col 2 lines 22-32).

22. Regarding claim 25, Hobbs discloses a multi-threaded system comprising: thread execution logic for generating instruction requests from an executing thread (col 2 lines 3-6); and threshold interrupt logic for generating an interrupt threshold value, wherein the thread execution logic only accepts interrupts having an interrupt priority higher than the interrupt threshold value (col 2 lines 54-57).

23. Regarding claim 26, Hobbs discloses the multi-threaded system of claim 25, further comprising interrupt thread logic for switching execution to a selected interrupt thread before servicing any interrupt (col 2 lines 67 to col 3 line 3).

24. Regarding claim 29, Hobbs discloses a multi-threaded system comprising: means for specifying an interrupt threshold value; and means for processing a

requested interrupt only when an interrupt priority value of the requested interrupt is higher than the interrupt threshold value (col 2 lines 54-57).

25. Regarding claim 30, Hobbs discloses the multi-threaded system of claim 29, wherein the means for processing the requested interrupt comprises: means for identifying one of the plurality of active threads as an interrupt thread (col 2 lines 3-6); means for switching to the interrupt thread if the interrupt thread is not executing (col 2 line 67 to col 3 line 3); and means for branching to the ISR (col 2 lines 12-15).

26. Regarding claim 31, Hobbs discloses the multi-threaded system of claim 30, wherein the means for processing the requested interrupt further comprises means for saving a thread context of the interrupt thread (col 1 lines 57 to 63).

27. Regarding claim 32, Hobbs discloses the multi-threaded system of claim 31, wherein the means for processing the requested interrupt further comprises means for restoring the thread context of the interrupt thread after executing a return from exception (RFE) instruction (col 2 lines 14 to 19).

28. Regarding claim 34, Hobbs discloses the multi-threaded system of claim 29, further comprising means for processing traps (col 3 lines 7-11), the means for processing traps comprising: means for detecting a trap from an originating thread (col 3 lines 40-46); means for storing trap background data for the trap if the trap is

asynchronous (col 3 lines 24-29); means for processing the trap if the originating thread is executing (col 3 lines 40-50); and means for associating a trap pending indicator with the originating thread if the originating thread is not executing (col 3 lines 40-50).

Note in line 44 the use of the term "delay". This suggests that there is an indicator waiting for a change to the originating thread.

29. Regarding claim 35, Hobbs discloses the multi-threaded system of claim 34, wherein the means for processing traps further comprises means for detecting execution of an active thread associated with the trap pending indicator (col 3 lines 40-50).

Note that, clearly, for the AST to throw and interrupt when its originating thread is being executed, that state must be detected.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 6-8, 17-19, 27-28, 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs (U.S. Patent No. 5,197,138) in view of Radhakrishna (U.S. Patent No. 6,823,414).

32. Regarding claim 6, Hobbs discloses the method of claim 5, wherein performing the interrupt entry process further comprises thread switching (col 2 line 67 to col 3 line 3).

Hobbs fails to disclose disabling interrupts.

Radhakrishna (U.S. Patent No. 6,823,414) discloses an ISR that disables interrupts (col 1 lines 66-67).

In the environment of Hobbs, a system with the intention of organizing a large number and type of interrupts by giving them a priority system, one of ordinary skill in the art would be motivated to allow for an interrupt that is already in the ISR to maintain it's priority rather than potentially being "interrupted" by a further interrupt. As shown in Radhakrishna col 1 line 67 to col 2 line 4, interrupts are disabled "so that the currently-interrupting event can be processed in an unbroken fashion (i.e., without further interrupts from the same device that diverts CPU processing attention before the ISR has completed it's function)."

It would have been obvious for one of ordinary skill in the art to allow the computer system of Hobbs to include the ability to disable interrupts while executing the ISR, as in Radhakrishna.

33. Regarding claim 7, Hobbs/Radhakrishan discloses the method of claim 6, wherein performing the interrupt exit process further comprises enabling interrupts (Radhakrishna col 2 lines 2-4)

Note that the interrupts are disabled so interrupts can not divert the "CPU processing attention before the ISR has completed its function", clearly suggesting that interrupts will be re-enabled after the ISR has completed.

And thread switching (col 2 lines 8-19).

Note that the term "writes in memory contents to registers" suggests a contrext switch (or thread switch).

34. Regarding claim 8, Hobbs/Radhakrishan discloses the method of claim 6, wherein executing the ISR comprises enabling interrupts (Radhakrishna col 2 lines 2-4) and thread switching (col 2 lines 8-19) after a predetermined interval (col 2 lines 12-14).

Note that the complete ISR program code is considered to be the predetermined interval.

35. Regarding claim 17, Hobbs/Radhakrishan discloses the method of claim 16, wherein performing the trap entry process further comprises disabling interrupts (103 with R from claim 6) and thread switching (col 2 line 67 to col 3 line 3).

36. Regarding claim 18, Hobbs discloses the method of claim 17, wherein performing the trap exit process further comprises enabling interrupts (Radhakrishna col 2 lines 2-4)

Note that the interrupts are disabled so interrupts can not divert the "CPU processing attention before the ISR has completed its function", clearly suggesting that interrupts will be re-enabled after the ISR has completed.

And thread switching (col 2 lines 8-19).

Note that the term "writes in memory contents to registers" suggests a contrext switch (or thread switch).

37. Regarding claim 19, Hobbs/Radhakrishan discloses the method of claim 17, wherein executing the trap handling routine comprises enabling interrupts (Radhakrishna col 2 lines 2-4) and thread switching (col 2 lines 8-19) after a predetermined interval (col 2 lines 12-14).

Note that the complete ISR program code is considered to be the predetermined interval.

38. Regarding claim 27, Hobbs/Radhakrishan discloses the multi-threaded system of claim 26, further comprising disabling logic for disabling interrupts and thread switching while an interrupt is being serviced (103 with R from claim 6).

39. Regarding claim 28, Hobbs/Radhakrishan discloses the multi-threaded system of claim 27, further comprising thread tagging logic for storing trap background data for asynchronous traps (col 3 lines 7-10 and col 3 lines 24-29), wherein every trap is handled in its originating thread (col 3 lines 40-50).

40. Regarding claim 33, Hobbs/Radhakrishan discloses the multi-threaded system of claim 32, wherein the means for processing the requested interrupt further comprises means for disabling interrupts (103 with R from claim 6) and thread switching (col 2 line 67 to col 3 line 3) during execution of the ISR (col 2 lines 12-14).

41. Regarding claim 36, Hobbs/Radhakrishan discloses the multi-threaded system of claim 35, wherein the means for processing the trap comprises means for disabling interrupts (103 with R from claim 6) and thread switching (col 2 line 66 to col 3 line 4 and col 3 lines 40-50).

Note that, as indicated in col 3 lines 15-20, the trap throws an interrupt, suggesting that it is treated as an interrupt.

Response to Arguments

42. Applicant's arguments filed May 8th, 2006 have been fully considered but they are not persuasive.

43. Applicant states:

"With respect to claims 1, 25, 29, the Office Action cites Hobbs at column 2, lines 54-57, to anticipate the 'interrupt threshold value' limitation. The cited portions of Hobbs do not teach, or even suggest, this limitation. In the cited portions, Hobbs merely

teaches that an interrupt will not be recognized or serviced by the processor until the priority of the code thread is lower than the priority of the interrupt...Hobbs does not even suggest 'processing a request interrupt only when [the/an] interrupt priority value of the requested interrupt is higher than the interrupt threshold value."

Examiner disagrees. It is unclear why Applicant believes that the claimed invention and Hobbs are not analogous. Examiner asserts that the "priority of the interrupt" is considered to be the "interrupt priority value" and the "priority of the code thread" is considered to be the "interrupt threshold value".

44. Applicant states:

"Claim 24 explicitly requires "processing traps only in the active threads originating the traps." In rejecting this limitation, the Examiner cites col 2 lines 22-32 of Hobbs. The cited portion of Hobbs merely defines a trap, it does not teach the above-mentioned limitation in claim 24."

Examiner disagrees. Note Hobbs col 1 lines 57-63 discussing the technique of switching threads, which requires replacing all of the register values. Also, "an exception that occurs after the end of an instruction is called a 'trap'". If the trap occurs, and the trap occurs immediately afterward, then the trap is processed in the active thread that originated the trap."

Conclusion

45. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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